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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,193	08/18/2003	Azeez Bhavnagarwala	YOR920030289US1 (8728-635	3651

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F. CHAU & ASSOCIATES, LLC
130 WOODBURY ROAD
WOODBURY, NY 11797

EXAMINER	
WEST, JEFFREY R	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/643,193	BHAVNAGARWALA ET AL.	
	Examiner	Art Unit	
	Jeffrey R. West	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19 and 26-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16,18,19 and 26-33* is/are rejected.

7)☒ Claim(s) *17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 May 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because of the following informalities:

Figures 8 and 9 are objected to because they do not contain descriptive titles. It is suggested that Applicant include titles to the graphs reflecting the information they present, specifically, on page 34, lines 12-17 and page 35, lines 4-9.

2. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 6-10, 12, 19, 26-29, and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Bastos et al., "Mismatch characterization of small size MOS transistors".

Bastos discloses a method for characterizing device mismatch in a semiconductor integrated circuit (page 271, column 1, "Introduction", lines 1-2), comprising the steps of obtaining DC voltage characteristic data (i.e. DC drain current based on DC gate voltage) for a pair of semiconductor devices by varying a transistor input gate voltage (page 271, column 2, "Measurement Methodology", lines 6-18 and page 272, column 1, "The Extraction Algorithms", lines 13-15), processing the DC voltage characteristic data to determine a distribution of device mismatch between devices comprising the device pair (page 272, columns 1-2, "The Extraction Algorithms", lines 1-15 and 32-36), determining a threshold voltage variation of the transistors in the integrated circuit using one or more determined distributions of mismatch for selected device pairs (page 272, column 2, "Algorithm

Validation", lines 1-16), and characterizing random variations of the integrated circuit (i.e. random variations in transistor dimensions) using one or more determined threshold voltage variations of transistors of the integrated circuit (page 274-275, "Mismatch Dependence on Transistor Size").

Bastos discloses that the device pair comprises two neighboring, similar, transistors (page 272, column 1, "The Extraction Algorithms", lines 13-15) and that the distribution of device mismatch comprises a distribution of threshold voltage mismatch (page 272, columns 1-2, "The Extraction Algorithms", lines 1-15 and 32-36).

Bastos discloses that the step of obtaining DC voltage characteristic data for the device pair comprises separately measuring DC voltage characteristic data for each of a plurality of similar device pairs (page 271, column 2, "Measurement Methodology", lines 5-6) and determining a variation in a device characteristic for a device of an integrated circuit comprising the device pair (page 274-275, "Mismatch Dependence on Transistor Size") as well as assessing random variation of device mismatch of the semiconductor integrated circuit using variations in the device characteristic for each of a plurality of devices of the integrated circuit as determined from repeatedly determining distributions of variation of device mismatch for device pairs within the integrated circuit (page 271, "The Test Chip" and page 272, column 2, "Algorithm Validation", lines 11-19).

Bastos also discloses that the distribution of threshold mismatch between the first and second transistors is between first and second NFETs (page 272, column 2, "Algorithm Validation", lines 11-14).

Bastos discloses that the step of determining a voltage threshold variation of transistors in the integrated circuit comprises determining a standard deviation of voltage threshold variation of the transistors (page 272, column 2, "Algorithm Validation", lines 1-16)

Bastos further discloses a plurality of programmed algorithms for execution by a test system and therefore it is considered inherent that some type of program storage device readable by the test system tangibly embodying the algorithms is present (page 271, column 2, "Measurement Methodology", lines 1-2 and page 272, column 1, "The Extraction Algorithms", lines 1-3).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bastos in view of U.S. Patent No. 6,731,916 to Haruyama.

As noted above, the invention of Bastos teaches many of the features of the claimed invention and while Bastos does obtain DC voltage characteristic data for a pair of transistors, Bastos does not specify retrieving this data from a database.

Haruyama teaches a power amplifying apparatus for a mobile phone including an FET with a bias current setting circuit (column 3, lines 9-11) and a memory/database (column 3, lines 11-13) wherein voltage characteristic data for the FET is stored in the memory/database (column 3, lines 14-20) and, when needed, is retrieved from the memory/database (column 3, lines 42-47).

It would have been obvious to one having ordinary skill in the art to modify the invention of Bastos to include retrieving the DC voltage characteristic data from a database, as taught by Haruyama, because Haruyama suggests that the combination would have saved time an effort by storing the characteristic data in a database (column 3, lines 14-20 and column 3, lines 42-47) thereby not requiring the process of measuring the characteristic data each time the mismatch is to be determined in the invention of Bastos.

7. Claims 5, 11, 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bastos in view of Conti et al., "Test structure for mismatch characterization of MOS transistors in subthreshold regime".

As noted above, the invention of Bastos teaches many of the features of the claimed invention and while Bastos does teach obtaining DC voltage characteristic

of a transistor pair, Bastos teaches obtaining the DC voltage characteristic for a transistor pair biased in the saturation region rather than the subthreshold region.

Conti teaches a test structure for threshold voltage mismatch comprising obtaining subthreshold DC voltage characteristic data for adjacent transistor devices (page 173, column 1, "Introduction, lines 1-9 and page 173, column 2, "Mismatch Model", lines 9-13) by biasing the transistors in a subthreshold region through application and maintenance of corresponding gate voltages (page 173, "Test Circuits" and page 174, column 1, lines 1-7).

It would have been obvious to one having ordinary skill in the art to modify the invention of Bastos to include obtaining the DC voltage characteristic for a transistor pair biased in the subthreshold region, as taught by Conti, because, as suggested by Conti, the combination would have improved the analysis of mismatch by providing a better estimates of threshold mismatch (page 174, column 1, lines 1-7).

8. Claims 13-16 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bastos in view of Conti and further in view of U.S. Patent No. 4,851,768 to Yoshizawa et al.

As noted above, the invention of Bastos and Conti teaches many of the features of the claimed invention, and while the invention of Bastos and Conti does teach biasing a transistor pair in a subthreshold region using proper varying gate voltages and obtaining a DC voltage characteristic of the transistor pair in order to determine threshold voltage mismatch for each of the transistor pairs, the combination does not

specify that the DC voltage characteristic is obtained by measuring an output voltage of a node between the first and second transistors and determining a distribution of input voltage for the given output voltage to determine the threshold voltage mismatch.

Yoshizawa teaches a characteristic test apparatus for an electronic device comprising a transistor pair configured with a node for measuring an output voltage, that varies as a function of the input voltage, between the first and second transistors (Figure 2a) wherein a varying/distribution of input voltages are applied to obtain voltage output to determine a threshold voltage as part of the DC voltage characteristic (column 4, lines 59-67 and column 6, lines 6-14).

It would have been obvious to one having ordinary skill in the art to modify the invention of Bastos and Conti to specify that the DC voltage characteristic is obtained by determining a distribution of input voltage for a given output voltage, as taught by Yoshizawa, because the invention of Bastos and Conti obtains a transistor characteristic to determine a threshold voltage and Yoshizawa suggests a similar method for determining such a transistor characteristic that would have simplified the characteristic determination by measuring two voltages, rather than requiring complex measurements of a current-voltage relationship, that, as suggested by Yoshizawa, would have complied with conventional means of measuring transistor characteristics using the input and output voltages (column 4, lines 59-68).

9. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over

Bastos in view of U.S. Patent No. 6,181,621 to Lovett.

As noted above, the invention of Bastos teaches many of the features of the claimed invention and while Bastos does teach characterizing mismatch in a semiconductor integrated circuit, Bastos does not specify that the integrated circuit be an SRAM.

Lovett teaches a threshold voltage mismatch compensated sense amplifier for SRAM memory arrays comprising means for obtaining threshold voltage mismatch information in a SRAM (column 1, lines 6-10 and column 2, lines 7-15).

It would have been obvious to one having ordinary skill in the art to modify the invention of Bastos to specify that the integrated circuit be an SRAM, as taught by Lovett, because Lovett suggests that SRAM devices are devices that are greatly affected by threshold mismatches due the size constraints of such SRAMs (column 3, line 65 to column 4, line 7) and therefore the combination would have provided greater utility in the invention of Bastos by applying the method to the SRAM devices.

Further, it has been held that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). In the instant case the structure of Bastos is capable

of characterizing transistor mismatch in any of a wide variety of integrated circuits, such as an SRAM, and therefore meets the claim.

Allowable Subject Matter

10. Claim 17 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims because none of the cited prior art teaches or suggests in combination with the other claimed limitations for characterizing device mismatch, applying a first gate voltage to a gate of a first transistor and a second gate voltage to a gate of a second transistor such that the first and second transistors are biased in a subthreshold voltage region, wherein at least one of the first and second gate voltage comprises a varying input voltage, determining a distribution of the input voltage for a given output voltage and determining a distribution of Vt mismatch of the transistors from the distribution of Vin corresponding to a distribution of one-half the Vt mismatch between the first and second transistors when the first and second transistors comprise an NFET and PFET.

Response to Arguments

11. Applicant's arguments filed May 02, 2005, have been fully considered but they are not persuasive.

Applicant first traverses the drawing objection asserting that "[t]here is no requirement to include descriptive titles, and the subject matter and information presented of Figs. 8 and 9 is abundantly clear from the specification."

The Examiner directs the applicant to 37 C.F.R. 1.84(o) which states, "[s]uitable descriptive legends may be used subject to approval by the Office, or may be required by the examiner where necessary for understanding of the drawing". Since the graphs do not explicitly state what information is being displayed, the Examiner requests descriptive legends for better understanding of the drawings. See MPEP 608.02.

With respect to the art rejections, Applicant argues, "[t]he inventions of claims 1, 10, 26 and 27 are generally directed to methods for characterizing device mismatch by processing DC *voltage* characteristic data of *pairs of semiconductor device* to determine a distribution of device mismatch between the semiconductor devices. Bastos is completely contrasted and opposite in teaching. Bastos teaches a method for characterizing of transistor mismatch by forming a test chip comprising a transistor array and then **independently measuring the drain current of each transistor in the array sequentially**. (See page 271). Clearly, Bastos does not disclose measuring *DC voltage characteristics,* much less *DC voltage characteristics of device pairs.* There is simply no reasonable basis for contending that Bastos teaches obtaining DC voltage characteristics for a transistor pair. In fact, the Examiner's reliance on Bastos in this regard is bewildering because Bastos teaches

nothing more then the conventional methods described in Applicants' specification related to FIG. 1, which Examiner requested by labeled 'Prior Art'."

The Examiner asserts that the claimed invention, as claimed in independent claim 1 for example, only requires obtaining DC voltage characteristic data for a device pair comprising semiconductor devices; and processing the DC voltage characteristic data to determine a distribution of device mismatch between the semiconductor devices." In this recitation, the data obtained is not clearly defined but only described as "DC voltage characteristic data".

Turning to the invention of Bastos, on page 272, column 1, Bastos indicates that "Four different algorithms are used to extract parameter mismatch values from the measured saturation region drain current I_D versus applied gate voltage V_{GS} curves of a pair of transistors."

The Examiner maintains that the curves of Bastos, which are measured from the transistor pair and comprise measured saturation drain current corresponding to measured and applied DC gate voltage values, are properly interpreted as "DC voltage characteristic data" since the curves include, and are a function of, the applied DC gate voltage. Further, the Examiner maintains that this section indicates that the DC voltage characteristic data is obtained for a transistor pair.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Shen et al., "Down Literal Circuit with Neuron-MOS Transistors and Its Applications" teaches a method for determining PMOS and NMOS threshold voltages and corresponding mismatch based on measured Vout vs Vin characteristics.

Lakshmikumar et al., "Characterization and Modeling of Mismatch in MOS Transistors for Precision Analog Design" teaches the determination of physical causes of mismatch for both p and n-channel devices.

Pavasovic et al., "Characterization of Subthreshold MOS Mismatch in Transistors for VLSI Systems" teaches the determination of subthreshold mismatch in transistor pairs.

Bhavnagarwala et al., "The Impact of Intrinsic Device Fluctuations on CMOS SRAM Cell Stability" teaches the determination of threshold voltage distribution functions for SRAM devices.

U.S. Patent No. 6,628,146 to Tam teaches a comparator circuit and method that determines a distribution of Vin for Vout of a transistor pair.

U.S. Patent No. 6,161,213 to Lofstrom teaches a system for providing an integrated circuit with a unique identification by plotting a distribution of threshold voltage mismatch between pairs of MOSFETs.

13. Applicant's amendment necessitated the new ground(s) of rejection presented in

this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey R. West whose telephone number is (571)272-2226. The examiner can normally be reached on Monday through Friday, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (571)272-2216. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jrw
July 25, 2005

MARC S. HOFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800